represents a packet re-reference value indicating a number of times a portion of a file, identified as a packet "i," is referenced during the time interval.

REMARKS

The Office Action mailed July 7, 1999, has been carefully considered.

In the Office Action, the Examiner repeated the objection to the title and the illegible oath signature. In addition, the Examiner rejected claims 21 and 22 under 35 U. S. C. §112, second paragraph, as being indefinate. The Examiner further rejected claims 1, 2, 17 and 18 under 35 U. S. C. §103 as being obvious over U. S. Patent No. 5,566,315 to Milillo et al. (hereinafter "Milillo") in view of U. S. Patent No. 5,590,308 to Shih (hereinafter "Shih"). The Examiner indicated that claims 3-16 and 19-24 were allowable (claims 21 and 22 being allowable after the correction of the deficiency under 35 U. S. C. §112, second paragraph).

Preliminarily, Applicant respectfully thanks the Examiner for the indication of allowable subject matter. By this amendment, Applicant is amending the title and claim 21 as required by the Examiner. Applicant respectfully submits that the title is sufficiently descriptive, and that claim 21 satisfies 35 U. S. C. §112, second paragraph. Applicant is obtaining a declaration from the inventor with (hopefully) a more legible signature, and will forward it when it is received.

Applicant respectfully submits that the claims patentably distinguish over the references. Applicant will first address claim 1 as representative. Claim 1 is directed to a system for generating an operational assessment of a cache memory in a digital data processing system for respective cache memory sizes comprising an operational statistics gathering element, a cache miss prediction element, and a cache memory size adjustment element. The operational statistics gathering element is configured to gather operational statistics over a time interval, including a file information retrieval activity value and an extent of activity value for each file accessed during the time interval. The cache miss prediction element is configured to generate a cache miss prediction value in response to the operational statistics gathered by the operational statistics gathering element and a cache memory size value. The cache memory size adjustment element configured to adjust the cache

memory size in response to the cache memory size value generated by the cache miss prediction element for a selected one of said cache miss prediction values.

Milillo describes a system for predicting and controlling the use of a cache memory in a computer system. Milillo's system adjusts the size of a cache memory based on two statistics gathered over various time periods, namely, an allocation rate and a blockage rate. As described in column 6, line 45 through column 7, line 10, the allocation rate is related to cache hits and the blockage rate is related to cache misses over respective time periods. Based on the allocation rates and blockage rates gathered over several diverse time periods, an allocation predictor and blockage predictor is generated, the diverse time periods essentially serving to provide filtering. Using the predictors, thresholds are generated which are used in releasing cache memory space. As described in Milillo, the threshold values are generated using only the cache hits and misses; there is no suggestion in Milillo of generating a cache miss prediction value based on operational statistics including a file information retrieval activity value and an extent of activity value for each file accessed during the time interval, and a cache memory size value, as required in the claim.

The Examiner contends at page 3, paragraph 5, second bullet, of the Office Action, that Milillo teaches generating generating a cache miss prediction value based on operational statistics including a file information retrieval activity value and an extent of activity value for each file accessed during the time interval at the top of column 14. Applicant respectfully disagrees. As described in the specification (page 9, lines 2-9), the file information retrieval activity value, represented by A_i, relates to the number of times the host computers issued requests to retrieve information from the particular "i-th" file, and the extent of activity, represented by E_i, relates to to the amount of the "i-th" file which is active. Neither of the statistics is derived from cache hit or cache miss statistics. Column 14 describes a high and low thresholds that the patent refers to as a "window of inactivity" between releasing cache space and ceasing the release of cache space. As is described in connection with FIG. 11, Milillo's system initially releases cache space if the amount of cache space used is above a low threshold, and will thereafter continue to release cache space if and while the amount of used cache space remains above a high threshold. As described in connection with FIGs. 9 and 10, the high threshold is the sum of an allocation predictor and a

blockage predictor, which are based on the allocation and blockage rates, respectively, and the low threshold is the sum of the high threshold and the blockage predictor. As is apparent, the "window of inactivity" is directly related to the blockage predictor, which, as noted above, is generated from the actual cache miss values over several time periods (to provide filtering). There is no suggestion of generating a cache miss prediction value based on operational statistics including a file information retrieval activity value and an extent of activity value for each file accessed during the time interval.

The Examiner apparently cited Shih for several deficiencies noted in connection with Milillo, namely, that Milillo does not disclose operational statistics and generating the cache miss prediction value based on a particular one of a plurality of cache memory management methodologies (the latter apparently related to claim 2). Shih describes an arrangement for reducing false invalidations in a distributed file system. In Shih's system, a distributed global cache memory LRU stack for a distributed file, multiple processor system is updated with local cache read hit data in accordance with a variable update interval. A global interval is determined for each processor as a function of statistical metrics from the most recent update interval. For large systems, in which the size of the global cache memory is much larger than the total size of the local cache memories, the update interval is the expected minimum residency time for a data record in the global cache memory. For small systems, in which the size of the global cache memory is approximately the same as the total size of the local cache memories, the updated interval is the expected average residency time in the local cache memories. In any case, while Shih discloses use of operational statistics in connection with a cache memory, there is no suggestion of use of operational statistics such as a file information retrieval activity value and an extent of activity value for each file accessed during the time interval, and a cache memory size value, as required in the claim.

The Examiner contends, at page 5, paragraph 6, first bullet, that Shih teaches use of file activity (namely, cache hits) collected over obervation intervals in statistics calculaitons that are used in his system. As noted above in connection with Milillo, however, this does not suggest the file information retrieval activity value and an extent of activity value recited in the claims.

Accordingly, Applicant respectfully submits that neither Milillo nor Shih, whether considered individually or in combination, teach or suggest the invention recited in claim 1.

Applicant further submits that independent method claim 9 and independent computer program product claim 17 are allowable for the reasons set forth above in connection with claim 1. Independent method claim 9 is directed to a method of generating an operational assessment of a cache memory in a digital data processing system using statistics along the lines of those set forth in claim 1. In addition, independent computer program product claim 17 is directed to a computer program product for enabling a computer to generate an operational assessment of a cache memory in a digital data processing system using statistics along the lines of those set forth in claim 1. Applicant further submits that dependent claims 2-8, 10-16 and 18-24 are allowable at least for the reason that they depend from allowable independent claims.

It is believed that this application is allowable, and a notice of allowability is respectfully solicited.

Respectfully submitted,

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